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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/707,844	11/08/2000	Hidetoshi Ishida	0819-448	9493
22204 7	590 12/05/2005		EXAMINER	
NIXON PEABODY, LLP 401 9TH STREET, NW			FARAHANI, DANA	
SUITE 900	221,1111		ART UNIT	PAPER NUMBER
WASHINGTO	N, DC 20004-2128		2891	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)	
	09/707,844	ISHIDA ET AL.	
Office Action Summary	Examiner	Art Unit	
	Dana Farahani	2891	
The MAILING DATE of this communication apperiod for Reply	opears on the cover sheet w	ith the correspondence address	·
A SHORTENED STATUTORY PERIOD FOR REP WHICHEVER IS LONGER, FROM THE MAILING I - Extensions of time may be available under the provisions of 37 CFR 1 after SIX (6) MONTHS from the mailing date of this communication If NO period for reply is specified above, the maximum statutory period Failure to reply within the set or extended period for reply will, by statu Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUN .136(a). In no event, however, may a d will apply and will expire SIX (6) MO tte, cause the application to become A	CATION. reply be timely filed NTHS from the mailing date of this communion BANDONED (35 U.S.C. § 133).	
Status			
1) Responsive to communication(s) filed on 23	September 2005.		
2a)⊠ This action is FINAL . 2b)☐ Th	is action is non-final.		
3) Since this application is in condition for allow	ance except for formal mat	ters, prosecution as to the meri	its is
closed in accordance with the practice under	Ex parte Quayle, 1935 C.I). 11, 453 O.G. 213.	
Disposition of Claims			
4) Claim(s) 11-16 is/are pending in the application	on.		
4a) Of the above claim(s) is/are withdra	awn from consideration.		
5) Claim(s) is/are allowed.			
6)⊠ Claim(s) <u>11-16</u> is/are rejected.			
7) Claim(s) is/are objected to.	(1 4)		
8) Claim(s) are subject to restriction and	ror election requirement.		
Application Papers			
9) The specification is objected to by the Examir	ner.		
10) ☐ The drawing(s) filed on is/are: a) ☐ ac			
Applicant may not request that any objection to the	*		
Replacement drawing sheet(s) including the corre			
Priority under 35 U.S.C. § 119			
12) ☐ Acknowledgment is made of a claim for foreig a) ☐ All b) ☐ Some * c) ☐ None of:		§ 119(a)-(d) or (f).	
1. Certified copies of the priority documer		N P P N -	
2. Certified copies of the priority documer		···	•
 Copies of the certified copies of the pri application from the International Bure 	•	r received in this National Stage	.
* See the attached detailed Office action for a lis		received.	
		.,	
Attachment(s)			
1) Notice of References Cited (PTO-892)		Summary (PTO-413)	
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/06 		(s)/Mail Date Informal Patent Application (PTO-152)	
Paper No(s)/Mail Date	6) Other:	<u> </u>	

DETAILED ACTION

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US Patent 5,151,770), newly cited.

Regarding claims 11 and 14, Inoue discloses in figure 1, a semiconductor device comprising:

A plurality of semiconductor elements, 24 and 26, formed on a semiconductor substrate 21; and

A plurality of through holes, which are provided between two adjacent ones of the plurality of semiconductor elements and pass from a surface through the backside of the semiconductor substrate 21, which is GaAs (see figure 5, and col. 9, lines 29-32. Note that the substrate should be 21 but has been indicated as substrate 1 in column 9).

Inoue does not expressly disclose a distance between two adjacent ones of the plurality of through holes (which is 100 microns. See col. 6, line 13) is smaller than a thickness of the semiconductor substrate. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the thickness of the substrate greater than 100 microns to have a solid support for the semiconductor

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device. See *In re Rose*, 105 USPQ 237 (CCPA 1955) for the proposition that a change in size is generally recognized as being within the level of ordinary skill in the art.

Regarding claim 12, the through holes are covered with a conductive material (see col. 8, lines 1-5).

Regarding claim 13, the conductive material is electrically connected to a ground wiring layer 52 (figs. 4 and 5) provided on the surface of the backside of the substrate (see col. 8, lines 1-5).

3. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue as applied to claims 11-14 above, and further in view of Nakamura et al., hereinafter Nakamura (US Patent 6,229,209), newly cited.

Inoue renders obvious the limitations in the claims, as discussed above, except for a second group of through holes which are provided in electrodes of the plurality of semiconductor elements, pass from a surface through the backside of the substrate, and whose faces are covered with conductive material.

Nakamura discloses in figure 1, a second group of through holes 23 which are provided in electrodes of the semiconductor element 3, pass from a surface through the backside of the substrate 20, and whose faces are covered with conductive material 24 (see col. 6, lines 4-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make connection to the semiconductor devices of the Inoue in the fashion of the Nakamura reference (which would lead to their connection to the backside ground wiring 52), commonly known as flip chip structure, in order to make contacts to the semiconductor components of the Inoue, and provide a

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ground voltage reference for those devices. Flip chip configurations and their advantages, such as occupying less space and making secure contacts are well known in the art.

Response to Arguments

4. Applicant'(s) arguments with respect to the previously rejected claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

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